

US Patent Application Serial No. 09/921,022
Amendment Dated 5/19/04
Reply to Office Action Dated 3/24/2004

Amendments to the Claims

The listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A method for reducing the slew rate of transition edges of a digital signal on ~~a node~~ an output node of an integrated circuit, comprising:

connecting a first switchably conductive device characterized by a first threshold voltage of a given polarity between said ~~node~~ output node of said integrated circuit and a voltage source, said first switchably conductive device having a control input connected to a first input signal to allow current conduction from said voltage source to said ~~node~~ output node of said integrated circuit when a voltage level of said first input signal is equal to and greater than said first threshold voltage and to disallow said current conduction when said voltage level of said first input signal is less than said first threshold voltage;

connecting a second switchably conductive device independent from said first switchably conductive device and characterized by a second threshold voltage of said given polarity greater than said first threshold voltage between said ~~node~~ output node of said integrated circuit and said voltage source, said second switchably conductive device having a control input connected to a second input signal to allow current conduction from said voltage source to said ~~node~~ output node of said integrated circuit when a voltage level of said second input signal is equal to and greater than said second threshold voltage and to disallow said current conduction when said voltage level of said second input signal is less than said second threshold voltage; and

connecting a driving signal as said first input signal of said first switchably conductive device and as said second input signal of said second switchably conductive device;

Docket No. 10010504-1
JJC 4050-003

US Patent Application Serial No. 09/921,022
Amendment Dated 5/19/04
Reply to Office Action Dated 3/24/2004

wherein said first switchably conductive device and said second switchably conductive device together operate to reduce the slew rate of transition edges of said output signal driven onto said output pad of said integrated circuit.

2. (Currently Amended) A method in accordance with claim 1, comprising:
connecting between said ~~node~~ output node of said integrated circuit and said voltage source one or more additional independent switchably conductive devices each characterized by a respective threshold voltage of said given polarity but different than said first threshold voltage, said second threshold voltage, and each other respective threshold voltage, each said one or more additional switchably conductive devices having a respective control input connected to a respective input signal to allow current conduction from said voltage source to said ~~node~~ output node of said integrated circuit when a voltage level of said respective input signal is equal to and greater than said respective threshold voltage and to disallow said current conduction when said voltage level of said respective input signal is less than said respective threshold voltage; and
connecting said driving signal as said respective input signal of said respective switch of each of said respective one or more additional switchably conductive devices;

wherein said first switchably conductive device, said second switchably conductive device, and said respective one or more additional independent switchably conductive devices together operate to reduce the slew rate of transition edges of said output signal driven onto said output pad of said integrated circuit.

3. (Currently Amended) An output driver that drives an output signal onto an output pad ~~apparatus for reducing the slew rate of transition edges of a digital signal on a node~~ of an integrated circuit, comprising:

a first switchably conductive device characterized by a first threshold

Docket No. 10010504-1
JJC 4050-003

US Patent Application Serial No. 09/921,022
Amendment Dated 5/19/04
Reply to Office Action Dated 3/24/2004

voltage of a given polarity, said first switchably conductive device ~~connected between said node~~ coupled between said output pad of said integrated circuit and a voltage source and having a control input connected to a driving signal to allow current conduction from said voltage source to said node output pad when a voltage level of said driving signal is equal to and greater than said first threshold voltage and to disallow said current conduction when said voltage level of said driving signal is less than said first threshold voltage; and

a second switchably conductive device independent from said first switchably conductive device characterized by a second threshold voltage of said given polarity greater than said first threshold voltage, said second switchably conductive device ~~connected between said node~~ coupled between said output pad of said integrated circuit and said voltage source and having a control input connected to said driving signal to allow current conduction from said voltage source to said node output pad when a voltage level of said driving signal is equal to and greater than said second threshold voltage and to disallow said current conduction when said voltage level of said driving signal is less than said second threshold voltage;

wherein said first switchably conductive device and said second switchably conductive device together operate to reduce the slew rate of transition edges of said output signal driven onto said output pad of said integrated circuit.

4. (Previously Presented) An apparatus in accordance with claim 3, wherein said first switchably conductive device comprises a single field effect transistor (FET) and single second switchably conductive device comprises a single field effect transistor (FET).

5. (Currently Amended) An apparatus in accordance with claim 3, comprising:

Docket No. 10010504.1
JJC 4050-003

US Patent Application Serial No. 09/921,022
Amendment Dated 5/19/04
Reply to Office Action Dated 3/24/2004

one or more additional independent switchably conductive devices each characterized by a respective threshold voltage of said given polarity but different than said first threshold voltage, said second threshold voltage, and each other respective threshold voltage, each said one or more additional independent switchably conductive devices connected between said ~~node~~ output pad and said voltage source and having a respective control input connected to said driving signal to allow current conduction from said voltage source to said ~~node~~ output pad when said voltage level of said driving signal is equal to and greater than said respective threshold voltage and to disallow said current conduction when said voltage level of said driving signal is less than said respective threshold voltage;

wherein said first switchably conductive device, said second switchably conductive device, and said respective one or more additional independent switchably conductive devices together operate to reduce the slew rate of transition edges of said output signal driven onto said output pad of said integrated circuit.

6. (Currently Amended). An apparatus in accordance with claim 5, wherein said first switchably conductive device comprises a single field effect transistor (FET) and single second switchably conductive device comprises a single field effect transistor (FET), and said one or more additional switchably independent conductive devices each comprises a single field effect transistor (FET).

7. (Currently Amended) A method for controlling the slew rate of transition edges of a digital signal on a ~~node~~ an output node of an integrated circuit, said method comprising the steps of:

driving, with a driving signal, a first switchably conductive device characterized by a first threshold voltage of a given polarity and connected between said ~~node~~ output node of said integrated circuit and a voltage source,

Docket No. 10010504-1
JJC 4050-003

US Patent Application Serial No. 09/921,022
Amendment Dated 5/19/04
Reply to Office Action Dated 3/24/2004

said first switchably conductive device having a control input connected to said driving signal to allow current conduction from said voltage source to said ~~node~~ output node of said integrated circuit when a voltage level of said driving signal is equal to and greater than said first threshold voltage and to disallow said current conduction when said driving signal is less than said first threshold voltage;

driving, with said driving signal, a second switchably conductive device independent from said first switchably conductive device characterized by a second threshold voltage of said given polarity greater than said first threshold voltage and connected between said ~~node~~ output node of said integrated circuit and said voltage source, said second switchably conductive device having a control input connected to said driving signal to allow current conduction from said voltage source to said ~~node~~ output node of said integrated circuit when said voltage level of said driving signal is equal to and greater than said second threshold voltage and to disallow said current conduction when said voltage level of said driving signal is less than said second threshold voltage.

8-11. (Canceled)

12. (Currently Amended) A method for reducing the slew rate of transition edges of a digital signal on a ~~node~~ an output node of an integrated circuit, comprising:

connecting a first switchably conductive device characterized by a first threshold voltage of a given polarity between said ~~node~~ output node of said integrated circuit and a voltage source, said first switchably conductive device having a control input connected to a first input signal to allow current conduction from said voltage source to said ~~node~~ output node of said integrated circuit when a voltage level of said first input signal is equal to and less than said first threshold voltage and to disallow said current conduction when said voltage level of said first input signal is greater than said first threshold voltage;

Docket No. 10010504-1
JJC 4050-003

US Patent Application Serial No. 09/921,022
Amendment Dated 5/19/04
Reply to Office Action Dated 3/24/2004

connecting a second switchably conductive device independent from said first switchably conductive device characterized by a second threshold voltage of said given polarity less than said first threshold voltage between said node output node of said integrated circuit and said voltage source, said second switchably conductive device having a control input connected to a second input signal to allow current conduction from said voltage source to said node output node of said integrated circuit when a voltage level of said second input signal is equal to and less than said second threshold voltage and to disallow said current conduction when said voltage level of said second input signal is greater than said second threshold voltage; and

connecting a driving signal as said first input signal of said first switchably conductive device and as said second input signal of said second switchably conductive device;

wherein said first switchably conductive device and said second switchably conductive device together operate to reduce the slew rate of transition edges of said output signal driven onto said output pad of said integrated circuit.

13. (Currently Amended) A method in accordance with claim 12, comprising:

connecting between said node output node of said integrated circuit and said voltage source one or more additional independent switchably conductive devices each characterized by a respective threshold voltage of said given polarity but different than said first threshold voltage, said second threshold voltage, and each other respective threshold voltage, each said one or more additional switchably conductive devices having a respective control input connected to a respective input signal to allow current conduction from said voltage source to said node output node of said integrated circuit when a voltage level of said respective input signal is equal to and less than said respective threshold voltage and to disallow said current conduction when said voltage level

Docket No. 10010504-1
JJC 4050-003

US Patent Application Serial No. 09/921,022
Amendment Dated 5/19/04
Reply to Office Action Dated 3/24/2004

of said respective input signal is greater than said respective threshold voltage;
and

connecting said driving signal as said respective input signal of said
respective switch of each of said respective one or more additional switchably
conductive devices;

wherein said first switchably conductive device, said second switchably
conductive device, and said respective one or more additional independent
switchably conductive devices together operate to reduce the slew rate of
transition edges of said output signal driven onto said output pad of said
integrated circuit.

14. (Currently Amended) An output driver that drives an output signal
onto an output pad apparatus for reducing the slew rate of transition edges of a
digital signal on a node of an integrated circuit, comprising:

a first switchably conductive device characterized by a first threshold
voltage of a given polarity, said first switchably conductive device connected
between said node output node of said integrated circuit and voltage source and
having a control input connected to a driving signal to allow current conduction
from said voltage source to said node output node of said integrated circuit when
a voltage level of said driving signal is equal to and less than said first threshold
voltage and to disallow said current conduction when said voltage level of said
driving signal is greater than said first threshold voltage; and

a second switchably conductive device independent from said first
switchably conductive device characterized by a second threshold voltage of said
given polarity less than said first threshold voltage, said second switchably
conductive device connected between said node output node of said integrated
circuit and said voltage source and having a control input connected to said
driving signal to allow current conduction from said voltage source to said node
output node of said integrated circuit when a voltage level of said driving signal is
equal to and less than said second threshold voltage and to disallow said current

Docket No. 10010504-1
JJC 4050-003

US Patent Application Serial No. 09/921,022
Amendment Dated 5/19/04
Reply to Office Action Dated 3/24/2004

conduction when said voltage level of said driving signal is greater than said second threshold voltage;

wherein said first switchably conductive device and said second switchably conductive device together operate to reduce the slew rate of transition edges of said output signal driven onto said output pad of said integrated circuit.

15. (Previously Presented) An apparatus in accordance with claim 14, wherein said first switchably conductive device comprises a single field effect transistor (FET) and single second switchably conductive device comprises a single field effect transistor (FET).

16. (Currently Amended) An apparatus in accordance with claim 14, comprising:

one or more additional independent switchably conductive devices each characterized by a respective threshold voltage of said given polarity but different than said first threshold voltage, said second threshold voltage, and each other respective threshold voltage, each said one or more additional switchably conductive devices connected between said node output node of said integrated circuit and said voltage source and having a respective control input connected to said driving signal to allow current conduction from said voltage source to said node output node of said integrated circuit when said voltage level of said driving signal is equal to and less than said respective threshold voltage and to disallow said current conduction when said voltage level of said driving signal is greater than said respective threshold voltage;

wherein said first switchably conductive device, said second switchably conductive device, and said respective one or more additional independent switchably conductive devices together operate to reduce the slew rate of transition edges of said output signal driven onto said output pad of said integrated circuit.

Docket No. 10010504-1
JJC 4050-003

US Patent Application Serial No. 09/921,022
Amendment Dated 5/19/04
Reply to Office Action Dated 3/24/2004

17. (Previously Presented). An apparatus in accordance with claim 16, wherein said first switchably conductive device comprises a single field effect transistor (FET) and single second switchably conductive device comprises a single field effect transistor (FET), and said one or more additional switchably conductive devices each comprises a single field effect transistor (FET).

18. (Currently Amended) A method for controlling the slew rate of transition edges of a digital signal on a node an output node of an integrated circuit, said method comprising the steps of:

driving, with a driving signal, a first switchably conductive device characterized by a first threshold voltage of a given polarity and connected between said node output node of said integrated circuit and a voltage source, said first switchably conductive device having a control input connected to said driving signal to allow current conduction from said voltage source to said node output node of said integrated circuit when a voltage level of said driving signal is equal to and less than said first threshold voltage and to disallow said current conduction when said driving signal is greater than said first threshold voltage;

driving, with said driving signal, a second switchably conductive device independent from said first switchably conductive device characterized by a second threshold voltage of said given polarity less than said first threshold voltage and connected between said node output node of said integrated circuit and said voltage source, said second switchably conductive device having a control input connected to said driving signal to allow current conduction from said voltage source to said node output node of said integrated circuit when said voltage level of said driving signal is equal to and less than said second threshold voltage and to disallow said current conduction when said voltage level of said driving signal is greater than said second threshold voltage;

wherein said first switchably conductive device and said second switchably conductive device together operate to reduce the slew rate of

Docket No. 10010504-1
JJC 4050-003

US Patent Application Serial No. 09/921,022
Amendment Dated 5/19/04
Reply to Office Action Dated 3/24/2004

transition edges of said output signal driven onto said output pad of said integrated circuit.

19. (Currently Amended) An output driver that drives an output signal onto an output pad ~~apparatus for reducing the slew rate of transition edges of a digital signal on a node~~ of an integrated circuit, comprising:

a first field effect transistor (FET) device characterized by a first threshold voltage of a given polarity, said first FET device having a source connected to a voltage source, a drain connected to said ~~node~~ output node of said integrated circuit, and a gate coupled to a driving signal; and

a second FET device characterized by a second threshold voltage of said given polarity and different than said first threshold voltage, said second FET device having a source connected to said voltage source, a drain connected to said ~~node~~ output node of said integrated circuit, and a gate coupled to said driving signal.

20. (Currently Amended) A method for reducing the slew rate of transition edges of a digital signal on a ~~node~~ an output node of an integrated circuit, comprising:

connecting a source of a first field effect transistor (FET) device to a voltage source, a drain of said first FET to said ~~node~~ output node of said integrated circuit, and a gate of said first FET to a driving signal, said first FET characterized by a first threshold voltage of a given polarity; and

connecting a source of a second field effect transistor (FET) device to said voltage source, a drain of said second FET to said ~~node~~ output node of said integrated circuit, and a gate of said second FET to said driving signal, said first FET characterized by a second threshold voltage of said given polarity but different than said first threshold voltage;

Docket No. 10010504-1
JJC 4050-003

US Patent Application Serial No. 09/921,022
Amendment Dated 5/19/04
Reply to Office Action Dated 3/24/2004

wherein said first field effect transistor (FET) and said second field effect transistor (FET) together operate to reduce the slew rate of transition edges of said output signal driven onto said output pad of said integrated circuit.

21. (Currently Amended) A method for controlling the slew rate of transition edges of a digital signal on ~~a node~~ an output node of an integrated circuit, said method comprising the steps of:

driving a gate of a first field effect transistor (FET) device with a driving signal, said first FET device characterized by a first threshold voltage of a given polarity and having a source connected to voltage source and a drain connected to said ~~node~~ output node of said integrated circuit; and

driving a gate of a second field effect transistor (FET) device with a driving signal, said second FET device characterized by a second threshold voltage of said given polarity and different than said first threshold voltage and having a source connected to voltage source and a drain connected to said ~~node~~ output node of said integrated circuit;

wherein said first field effect transistor (FET) and said second field effect transistor (FET) together operate to reduce the slew rate of transition edges of said output signal driven onto said output pad of said integrated circuit.

Docket No. 10010504-1
JJC 4050-003